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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,722	06/15/2001	Robert Roy Clarkson	5431.12-1	9180

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EXAMINER	
NORRIS, JEREMY C	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,722	CLARKSON ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *10-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of group I, claims 1-9 and 14-18 in Paper No. 4 is acknowledged. The traversal is on the ground(s) that a) the restriction is not proper "for not meeting the search burden requirement set forth in the M.P.E.P., and b) the restriction misinterprets the meaning of "independent and distinct". This is not found persuasive because, addressing point a), the M.P.E.P., is clear in outlining the requirements for showing a serious burden on the Examiner (see § 803 under the heading "**GUIDELINES**". In the previous Office Action, the Examiner has stated how the groups are differently classified. Applicant has not rebutted this showing by Examiner, therefore the traversal on this grounds is deemed unsuccessful. Regarding point b), Examiner refers Applicant to M.P.E.P § 802.01 for a discourse on the evolution of the interpretation of the phrase "independent and distinct". Said section sufficiently rebuts Applicant's argument. Therefore, the traversal on this grounds is also deemed unsuccessful.

The requirement is still deemed proper and is therefore made FINAL.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The

abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because of the use of the phrase "is provided". Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,285,086, granted to Sota et al. (hereafter Sota).

Sota discloses, referring to figures 1 and 2, a printed circuit board (5) having at least one mount area on a first surface thereof capable of having a microelectronic semiconductor device (1) coupled thereto, said mount area having a plurality of attach pads (7) on said first surface and a plurality of vias (9) extending from said first surface to a second surface of said printed circuit board, said printed circuit board comprising:

a plurality of collinear arrangements of vias, each of said collinear arrangements of vias including a respective first plurality of vias, each of said first plurality of vias being separated by a first distance from at least one adjacent via, said at least one adjacent via included in said first plurality of vias; and a plurality of collinear arrangements of attach pads, each of said collinear arrangements of attach pads including a respective first plurality of attach pads, each of said first plurality of attach pads being separated a second distance from at least one adjacent attach pad, said at least one adjacent attach pad included in said first plurality of attach pads, each of said collinear arrangements of attach pads being adjacently separated by a third distance from at least one of said first plurality of collinear arrangements of said vias, at least two of said first plurality of collinear arrangements of vias being adjacently separated by a fourth distance, and at least two of said first plurality of collinear arrangements of vias being adjacently separated by a fifth distance substantially equivalent to two times the fourth distance (all clearly understandable from figure 1) [claim 1], wherein said first distance and said second distance are equivalent [claim 2], wherein said third distance is substantially equal to one half said fourth distance [claim 3], wherein each of said first plurality of attach pads respectively included in each of said plurality of collinear arrangements of attach pads respectively provide an electrical contact for a lead of said microelectronic semiconductor device [claim 4], wherein said microelectronic semiconductor device is a ball grid array microelectronic semiconductor device [claim 5], wherein said microelectronic semiconductor device is a fine grid ball array semiconductor device [claim 6].

Claims 14-16 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,137,164, granted to Yew et al. (hereafter Yew).

Yew discloses, referring to figure 8, a printed circuit board (880) having at least one mount area for a microelectronic semiconductor device, said mount area comprising: a first subset of vias (832); and a second subset of vias (831) being spaced from said first subset of vias by a distance greater than a common inter-via distance between adjacent vias within each subset of vias, thereby defining an area unpopulated by said vias [claim 14], wherein the unpopulated area comprises a channel operable to accommodate at least one signal trace there through on a first surface of the printed circuit board (see col. 8, lines 15-30) [claim 15], wherein the unpopulated area is operable to accommodate at least one electronic circuit element on a second surface of the printed circuit board [claim 16], wherein a width of the unpopulated area is at least twice the common inter-via distance [claim 18].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sota in view of US 6,452,115, granted to Horiuchi et al (hereafter Horiuchi).

Sota discloses the claimed invention as described above with respect to claim 1, and further disclosing that the board is further comprising at least one signal trace on said first surface of said printed circuit board (see col. 4, lines 15-40). Sota does not specifically disclose that a portion of said at least one signal trace passing through said mount area, said portion being adjacent to at least two of said collinear arrangements of attach pads [claim 7]. However, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to route a signal trace in such a manner as said arrangement is well known in the art, as evidenced by Houriuchi (see figure 2, for example). The motivation for doing so would have been to allow communication with the interior pads.

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sota in view of US 6,222,246, granted to Mak et al. (hereafter Mak).

Sota discloses the claimed invention as described above except that Sota does not specifically disclose at least one capacitor mounted on said second surface of said printed circuit board on an area below said mount area [claim 8], wherein said capacitor is a decoupling capacitor operable to decouple power from at least one lead of said

microelectronic semiconductor device [claim 9]. However, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to so mount such a decoupling capacitor to the invention of Sota, as such an arrangement is well known in the art as evidence by Mak (see figure 2). The motivation for doing so would have been to have high decoupling capacitance and low inductance.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yew in view of Mak.

Yew discloses the claimed invention as described above with respect to claim 14, except Yew does not specifically state that the electronic circuit element is a decoupling capacitor operable to decouple power from leads of the microelectronic semiconductor device. However, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to so mount such a decoupling capacitor to the invention of Yew, as such an arrangement is well known in the art as evidence by Mak (see figure 2). The motivation for doing so would have been to have high decoupling capacitance and low inductance.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,441,493 Kim.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 703-306-

5737. The examiner can normally be reached on Mon.-Th., 9AM - 6:30 PM and alt. Fri. 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-0725 for regular communications and 703-308-0725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Albert W. Paladini 9-30-02

JCSN
September 29, 2002

ALBERT W. PALADINI
PRIMARY EXAMINER